



Design of a CMOS Comparator using Tanner Tool software

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ABSTRACT

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. In this research work, Design of a CMOS Comparator using Tanner Tool software is carried out.

Keywords: CMOS, RAM, COS-MOS, MOSFET.

I. INTRODUCTION

In 1963, while working for Fairchild Semiconductor, Frank Wanlass patented CMOS (US patent 3,356,858). Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts

when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct, while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time, both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

The image on the right shows what happens when an input is connected to both a PMOS transistor (top of diagram) and an NMOS transistor (bottom of diagram). When the voltage of input A is low, the NMOS transistor's channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output. Because the resistance between the supply voltage and Q is low, the voltage drop between the supply voltage and Q due to a current drawn from Q is small. The output therefore registers a high voltage.

On the other hand, when the voltage of input A is high, the PMOS transistor is in an OFF (high resistance) state so it would limit the current flowing from the positive supply to the output, while the NMOS transistor is in an ON (low resistance) state, allowing the output from drain to ground. Because the resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registering a low voltage.

In short, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behavior of input and output, the CMOS circuit's output is the inverse of the input.

The power supplies for CMOS are called VDD and VSS, or VCC and Ground (GND) depending on the manufacturer. VDD and VSS are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS, since both supplies are really source supplies. VCC and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS.

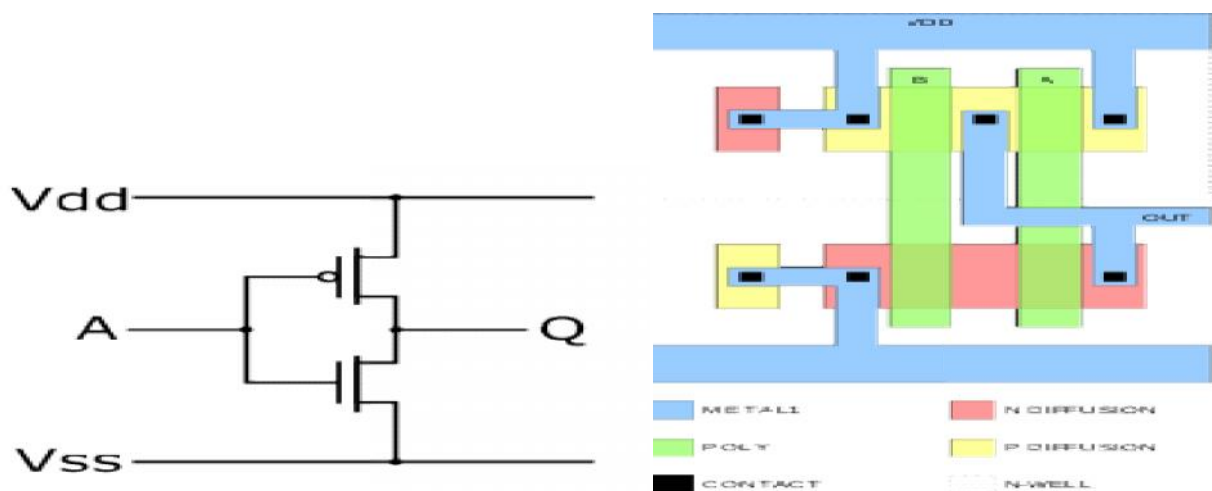


Fig 1: NAND gate in physical layout

The physical layout of a NAND circuit. The larger regions of N-type diffusion and P-type diffusion are part of the transistors. The two smaller regions on the left are taps to prevent latchup.

Simplified process of fabrication of a CMOS inverter on p-type substrate in semiconductor microfabrication. Note: Gate, source and drain contacts are not normally in the same plane in real devices, and the diagram is not to scale.

This example shows a NAND logic device drawn as a physical representation as it would be manufactured. The physical layout perspective is a "bird's eye view" of a stack of layers. The circuit is constructed on a P-type substrate. The polysilicon, diffusion, and n-well are referred to as "base layers" and are actually inserted into trenches of the P-type substrate. (See steps 1 to 6 in the process diagram below right) The contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1) making a connection.

The inputs to the NAND (illustrated in green color) are in polysilicon. The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N diffusion for the N device & P diffusion for the P device (illustrated in salmon and yellow coloring respectively). The output ("out") is connected together in metal (illustrated in cyan coloring). Connections between metal and polysilicon or diffusion are made through contacts (illustrated as black squares). The physical layout example matches the NAND logic circuit given in the previous example.

The N device is manufactured on a P-type substrate while the P device is manufactured in an N-type well (n-well). A P-type substrate "tap" is connected to VSS and an N-type n-well tap is connected to VDD to prevent latchup.

II. MOORE'S LAW

A plot of CPU transistor counts against dates of introduction; note the logarithmic vertical scale; the line corresponds to exponential growth with transistor count doubling every two years.

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years. The observation is named after Gordon E. Moore, the co-founder of Intel and Fairchild Semiconductor, whose 1965 paper described a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years.

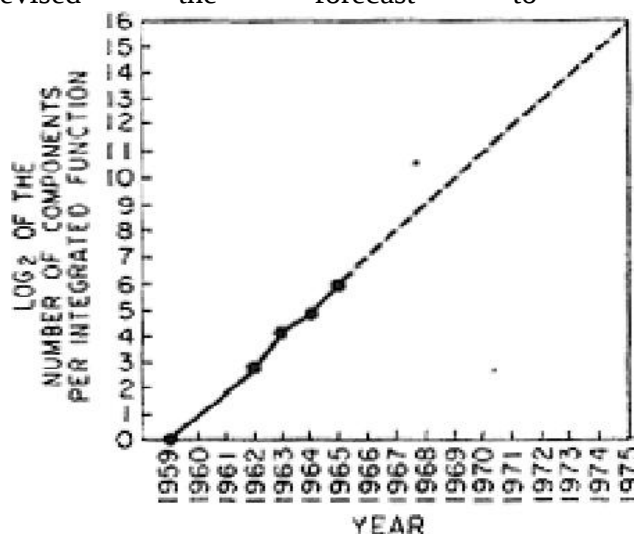


Fig 2 : Moore's Law

His prediction proved accurate for several decades, and the law was used in the semiconductor industry to guide long-term planning and to set targets for research and development. Advancements in digital electronics are strongly linked to Moore's law: quality-adjusted microprocessor prices, memory capacity, sensors and even the number and size of pixels in digital cameras.

Digital electronics have contributed to world economic growth in the late twentieth and early twenty-first centuries. Moore's law describes a driving force of technological and social change, productivity, and economic growth.

The period is often quoted as 18 months because of Intel executive David House, who predicted that chip performance would double every 18 months (being a combination of the effect of more transistors and the transistors being faster).

"Moore's law" should be considered an observation or projection and obviously not a physical or natural law. Although the rate held steady from 1975 until around 2012, the rate was faster during the first decade. In general, it is not logically sound to extrapolate from the historical growth rate into the indefinite future. For example, the 2010 update to the International Technology Roadmap for Semiconductors, predicted that growth would slow around 2013, and Gordon Moore in 2015 foresaw that the rate of progress would reach saturation: "I see Moore's law dying here in the next decade or so."

Intel confirmed in 2015 that the pace of advancement has slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nm. Brian Krzanich, CEO of Intel, announced that "our cadence today is closer to two and a half years than two." This is scheduled to hold through the 10 nm width in late 2017. He cited Moore's 1975 revision as a precedent for the current deceleration, which results from technical challenges and is "a natural part of the history of Moore's law."

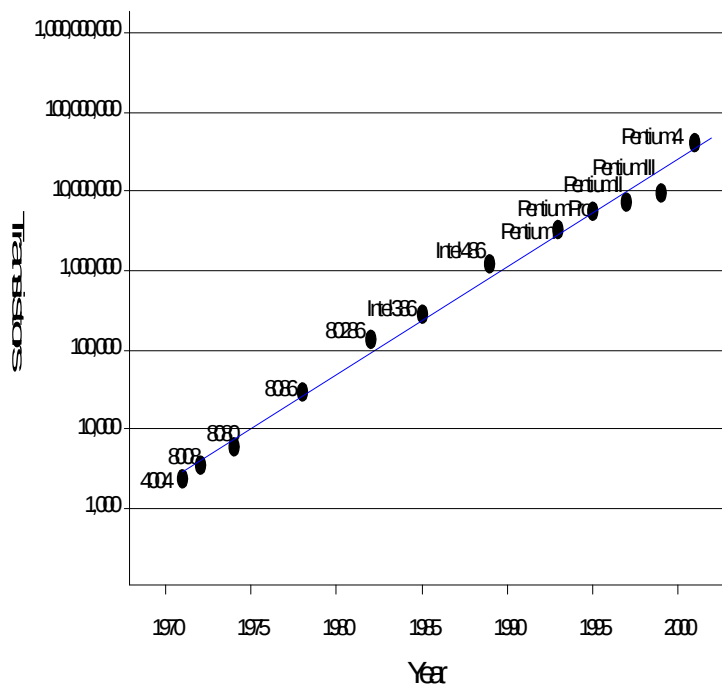


Fig 3 : Transistor counts have doubled every 26 months for the past three decades.

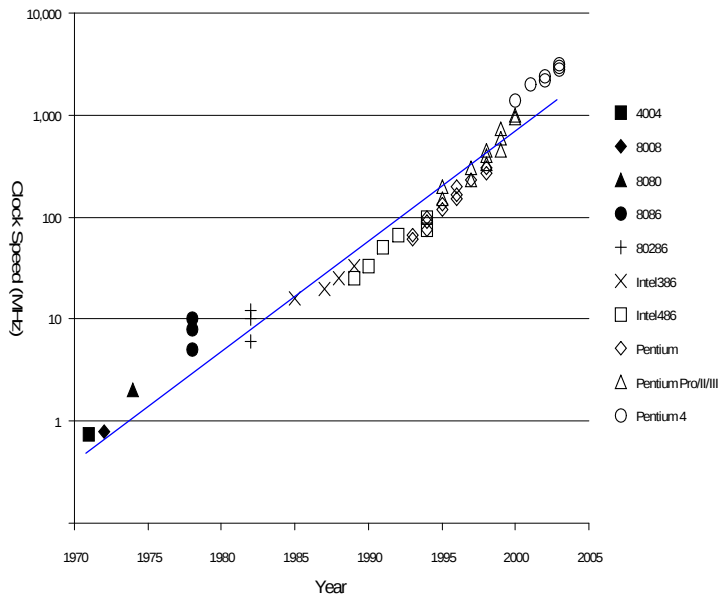


Fig 4 : Clock frequencies have also increased exponentially

III. CONCEPT OF COMPARATOR

Comparator is an important device widely used in Analog to Digital Converter (ADC). Among the many architectures of ADC, Sigma delta, designs are used in a large class of applications ranging from low frequency and audio to down converted intermediate frequency and digital video. Their property to Trade speed for accuracy makes them more attractive in the context of present CMOS technology evolution. Low power and high speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems. The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers. Comparators are used in ADCs, data transmission, switching power regulators, and many other applications.

The comparator design plays an important role in high speed ADCs. Power consumption & speed is key metrics in comparator design. For all high speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption. In a SDADCs, internal comparators are main building blocks for amplify small voltages into logic levels and the results are stored in the latch which will be used for conversion.

This comparator gives high speed & low power consumption for using in SDADCs design. Comparators can be divided into open-loop and regenerative comparators. The open loop comparators are basically op-amps without compensation. Regenerative comparators use positive feedback. Similar to sense amplifier or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast. This Design proposed the high speed & low power consumption comparators referred as an open loop comparators.

IV. COMPARATOR DESIGN

A comparator acts as the quantizer in the ADCs. Since the comparator is of 1-bit it has only two levels either a '1' or a '0'. A '1' implies that $V_{DD} = +2.5V$ and a '0' implies that $V_{SS} = -2.5V$.

If the input of the comparator is greater than the reference voltage (V_{ref}) it has to give an output of '1' and if the comparator input is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently. Given a reference level, a comparator gives an output of V_{DD} when the signal is greater than the reference level and an output of V_{SS} when signal is less than reference level. In this design the $V_{ref} = 0V$.

The operational amplifier can be used as a comparator. In this comparator design we have used the two stage CMOS OPAMP design technique for achieving high speed & low power consumption. Eliminated the compensation capacitor which will be used for designing a high gain two stage CMOS OPAMP topology and reduced the power consumption & increase speed in the presented design. Compensation capacitor is used in two stage CMOS OPAMP for providing stability in the design, compromise with stability to obtain the high performance as low power consumption with high speed. Present CMOS comparator design is shown in Fig.6.

This comparator consists by using current mirrors, current sinks, active load & constant current source. Transistor W/L ratios are as selected which gives accurate & optimum results. Parasitic effects which influences in the comparators performance is minimized in this design. This help to get the desired output for a high speed & low power consumption. Present Design has used ± 2.5 Volts power supply for simulation & designing. The comparator circuit as shown in Fig.5 has been simulated using T-SPICE with HP 0.5 technology.

Design of a CMOS Comparator for Low Power and High Speed

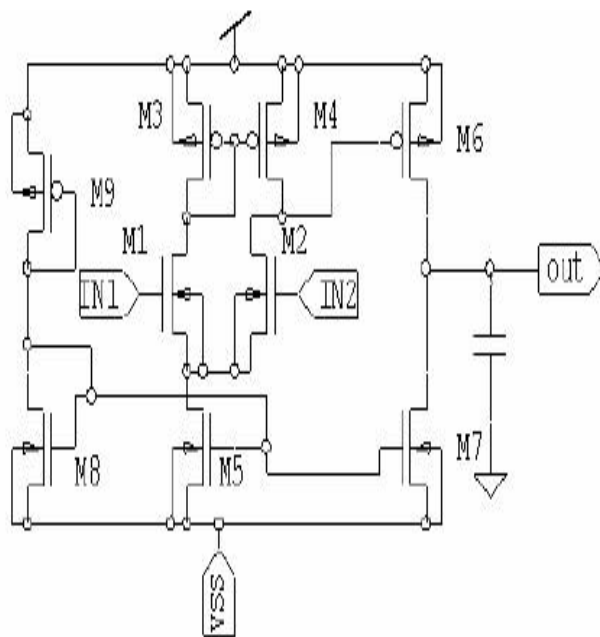


Figure 5: Proposed design of a CMOS comparator.

V. SIMULATION RESULTS & DISCUSSION

The simulation is done using Tanner EDA tool with HP 0.5 technology. We apply sinusoidal wave of 2.5 V amplitude with 5 kHz frequency on IN1 terminal and other terminal is grounded. Comparators perform the comparison for these inputs and we have obtained the response as square wave output and is presented in Fig.6. Generally comparators work as a one bit ADCs so the output response of comparator is used to evaluate the binary values for an analog output. All the simulated responses are reported for a period of 0.0002 sec to 0.001sec. Average power

consumption for this period (0.0002sec to 0.001sec) has been observed from net list output file and the output result is shown in Fig.8 and power consumption is about 0.31 mW.

The output results for power consumption are shown in Fig.8. Power consumption is the most important factor for designing a high performance comparator which will be used in SDADCs design. Speed of the reported design is obtained by apply the square wave of 2.5 V amplitude to IN terminal of the comparator. Obtained results are presented in Fig.8. The speed of the proposed design is measured by observing the difference between 50% rise of input & output waveform as shown. The speed of this design is 3.6 nano sec. Slew rate is 11.85 V/ μ s as shown in Fig. 9. We have compared present design results with earlier reported work and get improvement in the reported design and are shown.

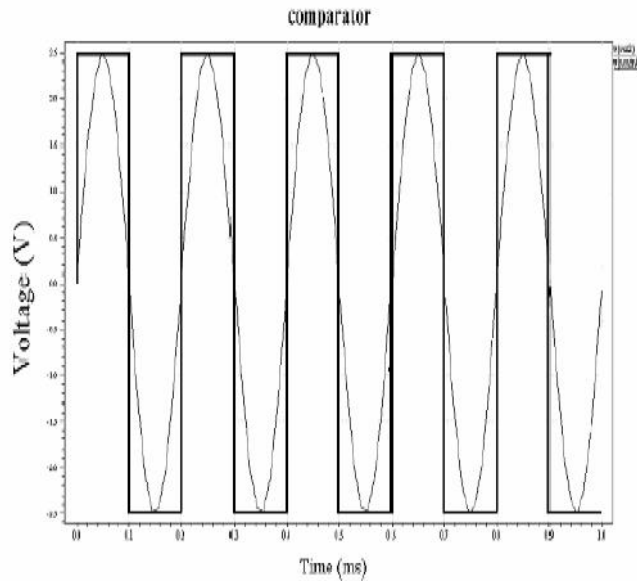


Figure 6: Output of Comparator for sinusoidal wave of 5 KHZ frequency.

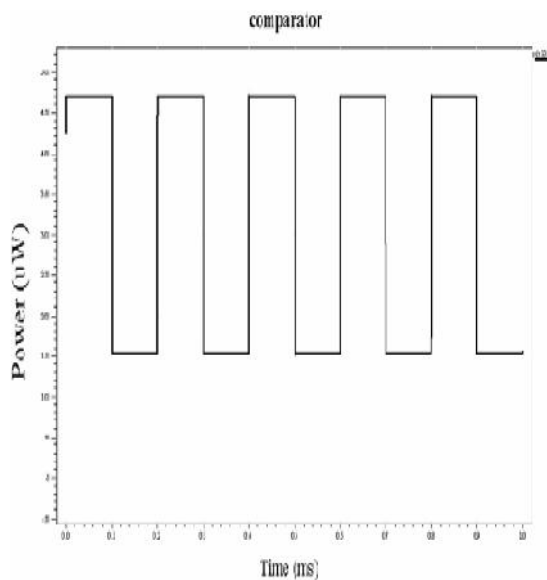
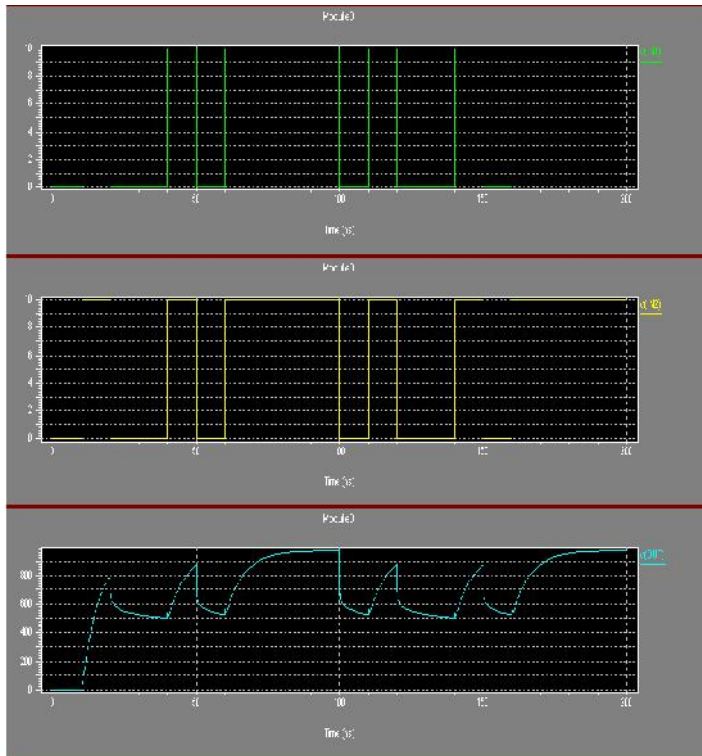


Figure 7: Present design results for power consumption.

Output Waveform



VI. APPLICATIONS & FUTURE SCOPE

A) Applications

- Null detectors
- Zero-crossing detectors
- Relaxation oscillator
- 5Level shifter
- Analog-to-digital converters
- Window detectors

B) Future Scope

- Current comparator
- Constant fraction discriminator
- Digital comparator
- Flash ADC
- List of LM-series integrated circuits
- Sorting network
- Zero crossing threshold detector

The nineties witnessed quantum leaps interface designing for improved man machine interactions. The BLUE EYES technology ensures a convenient way of simplifying the life by providing more delicate and user friendly facilities in computing devices. Now that we have proven the method, the next step is to improve the hardware. Instead of using cumbersome modules to gather information about the user, it will be better to use smaller and less intrusive units. The day is not far when this technology will push its way into your house hold, making you more lazy. It may even reach your hand held mobile device. Any way this is only a technological forecast.

VII. CONCLUSION

This Design has used the two stage CMOS OPAMP design technique generally it referred as an open loop comparators where we eliminate the compensation to achieved better performance. This comparator is designed for used in high resolution sigma delta ADCs. A simulation result is obtained by considering ± 2.5 V power supply. Here we achieved the high speed of 3.6 nano sec and power consumption of 0.31 mW.

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